reconsideration and allowance of independent claim 22 and its dependent claim 23 is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.41080X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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GEM/dlt

Called back @ 2:00PM on 3/[illegible] 05/05 - Voice mail already mailed will pick up - LEE

Left message 3/2/05 - Greg Montone he will call back

He never called back
Left message 3/8/05 @ 4:07pm.
If no message by 12:00 noon on 3/9/05 Do what is necessary.

APPENDIX A

PARTIAL ENGLISH TRANSLATION OF JP-A-53-10283

Scope of Claim for a Patent:

An MOS type semiconductor integrated circuit comprising a gate insulating film for a linear MOS transistor, said gate insulating film being obtained by using at least one member selected from the group consisting of hafnium oxide, aluminum oxide, tantalum oxide and niobium oxide.

① Page 438 right-hand lower column line 4 from the bottom to page 439 left-hand upper column line 4:

By the way, important thing for performance of the MOS transistor is, in the case of using an insulating film other than SiO_2 as the gate, to show C-V properties equivalent to almost ideal SiO_2-Si interface formed by thermal oxidation. Factors influencing the C-V properties are stabilization of the insulating film composition, strain, + charge of Na, K, etc. in the film, and the like. Thus, it is necessary that these conditions are sufficiently suitable.

② Page 439 left-hand upper column lines 5-16:

Next, properties of the gate insulating film of the present invention as examples are explained. Using N type 8.3 Ω-m silicon substrate, a HfO_2 film of 1000 Å thick was formed on the substrate using a reactive sputtering method.

According to this structure, since the film thickness became 1000 Å, its pressure tightness became 6×10^6 V/m or more to improve the pressure tightness remarkably. Further, electrical properties of this HfO_2 film (C-V properties of Si-HfO_2 series) are shown in Fig. 2. Fig. 2 shows a rate of the voltage Vs of the Si substrate side and change of normalized capacity, wherein the capacity change occurs at O_v

and almost ideal C-V properties are obtained, these properties being preferable as the MOS transistor.

③ Page 439 left-hand upper column lines 14-18:

As mentioned in above experimental results, the insulating film of the present invention is excellent in electrical properties. This seems to be derived from stability of the composition, less strains, no hygroscopicity and small content of charges of Na, K, etc.

⑲日本国特許庁　　⑪特許出願公開

公開特許公報　　昭53—10283

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審査請求　未請求

(全 4 頁)

⑤4MOS型半導体集積回路

⑪特　　願　昭51—84851
⑫出　　願　昭51(1976)7月15日
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明　　細　　書

1、発明の名称

MOS型半導体集積回路

2、特許請求の範囲

リニアMOSトランジスタのゲート絶縁膜として酸化ハフニウム，酸化アルミニウム，酸化タンタル，酸化ニオブのうち少くとも1つを用いたことを特徴とするMOS型半導体集積回路。

3、発明の詳細な説明

本発明はMOS型半導体集積回路に関し、リニア集積回路ICに適したMOSICを得ることを目的とする。

すなわち、本発明はリニアMOSICに適すると思われるいわゆるショートチャンネルMOSトランジスタの雑音性能の向上を目的とした構造を提供するものである。

近年、MOS集積回路の高密度化、高精度化が進みその中で、チャネル長を短かくしてショートチャネル化し、動作速度の向上、ファンアウトの向上などを合わせ適応するための検討が広く行なわれている。一方、MOS・ICのリニア(アナログ)ICへの適用ということで、オペアンプなど単純な回路から広範な回路応用への試開がなされており、その用途の1つはオーディオ分野である。オーディオ用としてのMOSICは、J-FET(ジャンクションFET)と比較しても数多くの利点もあるが、やはり最大の欠点は、雑音指数が大きいためと思われる。

ところで、MOSトランジスタの雑音に関しては、多くの理論的検討がなされてはいるが、最もよく知られた理論式としては、S.Christensson "Low Frequency Noise in MOS transistor" Solid State Electronics Vol11,1968 が出しているように

$$V^2gn = \frac{q^2}{C_{ox}\cdot W\cdot L}\, N_T \frac{\pi}{2\omega} \quad \cdots\cdots (1)$$

Vgn：入力換算雑音電圧
Cox：ゲート酸化膜容量
W,L：チャネル巾及び巾
N_T：トラップ密度

a：$\frac{2}{h}\sqrt{2m^*H}$　　H：ポテンシャルバリア

(1)式の様にあらわされ、チャネル巾の平方根に反比例し、ゲート酸化膜厚に反比例する。

前述したごとくMOS・ICのショートチャネル化によるgm(相互コンダクタンス)の向上によりバイポーラトランジスター並みの低いオン抵抗のものが実現されるようになり、オーディオ用を初めとするリニアMOSの登場があるにもかかわらず、(1)式に見られるように、チャネル長(セルフアラインで作った場合、ゲート巾と一致)を短かくすると、雑音が大きくなる欠点がある。

そこで、これらの欠点をなくすためにまず考えられることは雑音に反比例するゲート酸化膜容量Coxを大きくすべくゲート絶縁物を薄くし、あわせてショート・チャネル効果によるV_Tの低下をおさえることである。しかるに本発明者らの検討によると第1図に示すように、雑音電圧の目安となる入力換算雑音抵抗Rng(Ω)は素子の大きさ、ゲート酸化膜厚により非常に差が出てくる。たとえば、従来、低雑音として位置されているJ－FET(接合形FET)、低雑音バイポーラに比し、MOS Ⅰは優れており、MOS Ⅱは同程度、MOS Ⅲは劣る特性である。第1図のMOS Ⅰ，Ⅱ，Ⅲはすべて二酸化シリコンゲート絶縁膜を用いたもので、その膜厚tox，チャネル長，チャネル巾Wは次の如くである。

	tox	L	W
MOS Ⅰ	300Å	50μ	10,000μ
MOS Ⅱ	300Å	2μ	1,000μ
MOS Ⅲ	1,200Å	2μ	1,000μ

第1図から明らかなとおりMOS Ⅰは雑音抵抗は小さくリニアICにきわめて適した性能を有しているが、LもWも非常に広くWは1cmにもおよびしも50μであり集積化が不可能な寸法である。そして一番の問題は単位面積当り1.1×10^{-7}(F)の容量を有する酸化膜の膜厚tox＝300Åの場合その耐圧が最大10V程度と小さく、耐圧，劣化，歩留り低下などを含む信頼性および生産性の点で実用上満足すべきものが得にくいことである。また MOS Ⅱは酸化膜厚も十分厚く耐圧も高く、Lも2μとショートチャネルでありWも1000μと通常のMOS ICにおいてそれほど大きな寸法ではないか、雑音抵抗が著しく高く実用的ではない。さらに、前述のMOS Ⅱと同じで酸化膜厚toxが300Åと薄いMOS Ⅲは J－FETなみの性能を示し、L，Wの寸法もほぼ集積回路素子として適切であると考えられる。しかし、前述したように膜厚toxが300Åと薄く生産性および信頼性の点が最も大きい問題である。

そこで、本発明は以上の考察の結果、たとえばリニアICなどに要求される信頼性の高い低雑音MOSトランジスタを生産性良く実現しようとするもので、たとえば前述した二酸化シリコン(SiO_2)膜300Å(単位面積当りの容量1.1×10^{-7}(F))相当で十分耐圧の高い低雑音のショートチャネルMOSトランジスタを得るものである。

すなわち、本発明の特徴とする絶縁膜は、検討の結果MOSトランジスタのゲート絶縁膜として誘電率が高く厚くすることが可能で、より耐圧を高くすることができ、誘電率の高い他の物質に比しMOSトランジスタのゲート絶縁膜として使用できない特性すなわち水溶性であること、分離しやすいこと、生成が可能なことなどの検討の結果選ばれたものである。

この検討の結果選ばれた絶縁膜は、酸化ハフニウム(HfO_2)，酸化タンタル(Ta_2O_5)，酸化アルミ(Al_2O_3)，酸化ニオブ(Nb_2O_5)である。さて、HfO_2，Ta_2O_5，Al_2O_3，Nb_2O_5の比誘電率は11.7，27，9.0，32.5でありSiO_2に比べ極めて大きく従来よりMOSゲート絶縁特性として好ましい性質を有する。ところで、比誘電率が8.5以下の絶縁物を使用してもSiO_2膜との膜厚比もせいぜい2倍くらいであり、本発明の意図する低雑音，耐圧向上についてはとんどみるべき効果が得られなかった。

ところで、MOSトランジスタの性能にとって重要なことは、SiO_2以外の絶縁膜をゲートに用いた場合、熱酸化で形成された従来的なSiO_2－Si界面と等価なC－V特性を示すことである。こ

のC－V特性に影響する要因は絶縁膜組成の安定化，並，膜内におけるNa^+,K^+等の不純物等であり，これらの条件が充分達したものであることが必要である。

つぎに、本発明の実施例にかかるゲート絶縁膜の性質を説明する。N形0.3 Ω-mのシリコン基板を用いこの基板上に反応性スパッタリング法を用いて膜厚1,000Å のHfO_2膜を生成した。

この構成によれば膜厚も1,000Åとなった結果その耐圧も6×10^6V/m以上となり、著しい耐圧向上をはることができた。さらにこのHfO_2膜の電気的特性（Si-HfO_2系のC－V特性）を第2図に示す。第2図はSi基板側の電圧Vsと規格化した容量の変化の割合を示したもので、C_Vで容量変化が殆ど理想に近いC－V特性をはることができ、MOSトランジスタとして好ましい特性である。このHfO2膜を用いたMOSトランジスタは閾値電圧については第1図のMOSⅡとは同様の性能を示し、耐圧が向上し、リニア（アナログ）用途に好適である。

第3図はHfO_2に代えてTa_2O_5を用いたときのC－V特性を示し、第2図の場合と同じくN形1Ω-cmシリコン基板に1140Åの厚さのTa_2O_5膜を生成したものである。第3図の横軸は理論的に求めたTa_2O_5膜における理想特性を示し、実線は実験に測定したC－V特性である。この第3図から明らかなとおり、Ta_2O_5においても理想に近い電気的特性をはることができ、耐圧もHfO_2とほぼ同程度の性能をはることができた。

なお、Al_2O_3，Nb_2O_3についても誘電率が大きく、容易に生成可能で膜組成も比較的安定でゲート絶縁膜として十分適用可能であることがわかった。

このようにして、実験の結果上述した本発明にかかる絶縁膜の電気的特性がすぐれているのは、基板するに組成が安定で、塵が少なく、吸湿性がなく、Na^+等の不純物を含むことが少ないためであると思われるが、とにかく本発明にかかるゲート絶縁膜はシリコンチャネルでとくにリニアMOSトランジスタに適用して好ましい性能を有するものである。

なお、本発明にかかる高耐電圧ゲート絶縁膜は、スパッタリング，CVD法，電子ビーム蒸着法，金属の陽極酸化法，プラズマ分解法等により生成され得て、加工についてはリフトオフ法，ドライエッチング法などを用いることができる。

また本発明にかかる絶縁物とSiO_2膜を組合することによりさらに耐圧の改善をすることが出来る。たとえばSiO_2膜200Å，本発明にかかる絶縁膜500Å程度組合する。このように組合すれば、ピンホールを減少させることができ、さらに耐圧を向上させることができる。このピンホールが発生するのは、異なった大きさの原子又は分子状態の場合、そのピンホールを作る場所，密度が異なり、同じ酸化物であってもSiO_2中でのピンホールが出来る場所とその上の異種絶縁物膜のピンホール場所とが一致していないためである。

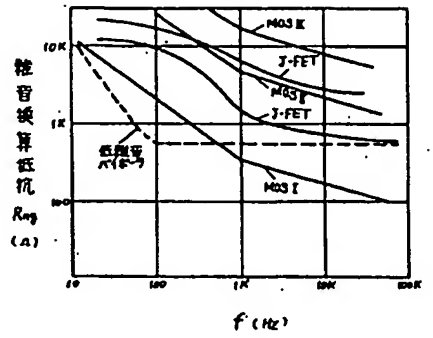
以上、述べて来たように、本発明は、シリコンチャネルMOSトランジスタにおける低電圧化について、従来の様子が著しく改善となり、生産性，信頼性が向上したものに対し、高耐圧化を達成することができMOS型ICの応用分野の拡大に大きく寄与するものである。

4．図面の簡単な説明

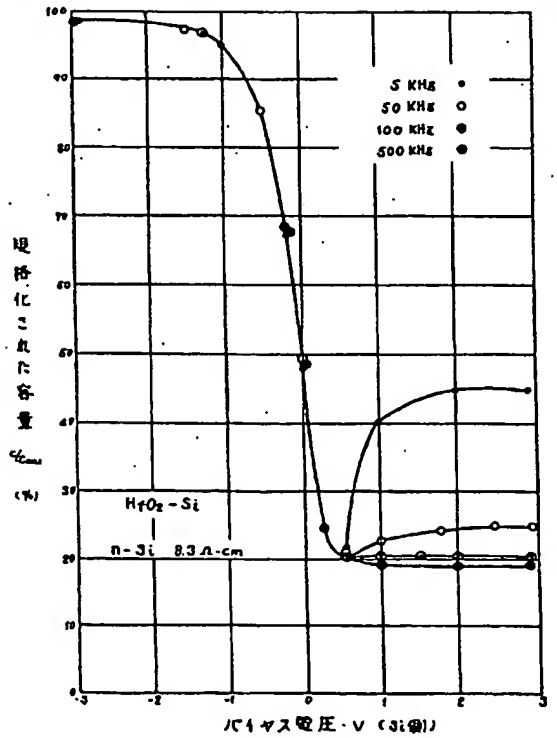
第1図は各素子（MOS，J－FET，バイポーラ素子）の動作領域と抵抗で比較図、第2図は本発明の一実施例にかかるHfO2-Si系の電圧－容量特性図、第3図は同Ta_2O_5-Si系の電圧－容量特性図である。

代理人の氏名　弁理士　中　尾　敏　男　ほか1名

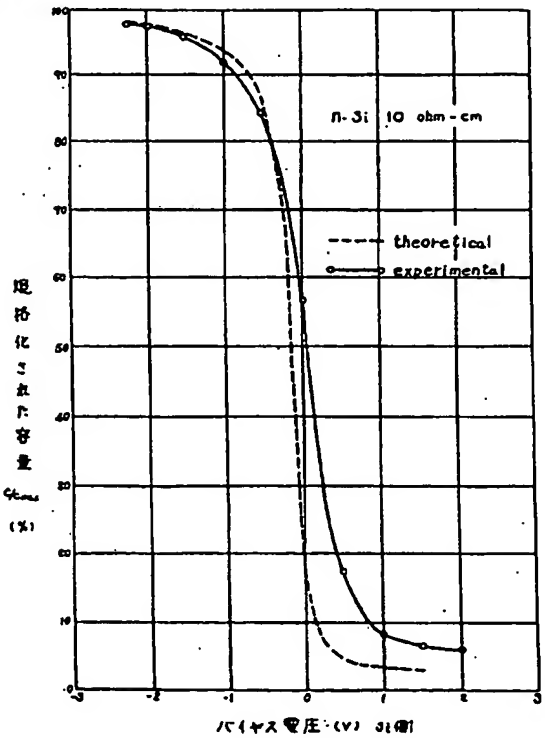
第 1 図



第 2 図



第 3 図



REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated August 24, 2004.

By the present Amendment, claim 25 and its dependent claims have been amended to express the features previously defined in terms of means plus function language as a "wherein clause" instead. Although Applicants respectfully submit that the previous means plus function language was clearly supported by the Specification, in order to expedite the allowance of this application, this terminology has been changed to a "wherein clause" to obviate the 35 U.S.C. § 112, second paragraph, rejection. Therefore, removal of this rejection is respectfully requested.

The remarks which follow are directed to the various prior art rejections set forth in the Office Action. Following an initial review of the following remarks, it is requested that the Examiner contact the undersigned attorney to schedule an interview to discuss the rejections. Applicants and the undersigned attorney greatly appreciate the Examiner's courtesy and cooperation in this regard.

Independent Claims 17, 18, 20, 24 and 25

Reconsideration and allowance of independent claims 17, 18, 20, 24 and 25, and their respective dependent claims, over the cited prior art to Matsushita (JPA 53-10283), Okada (USP 5582640), VanDover (USP 6093944) and Lau is respectfully requested. With regard to this, each of the independent claims 17, 18, 20, 24 and 25 contains the specific recitations that:

> "Compression strain is produced so that interatomic distances in the material are decreased to suppress leakage current from flowing through the gate insulators."

It is respectfully submitted that nothing in the primary reference to Matsushita, whether considered alone or in combination with the other cited prior art to Okada, VanDover and Lau, teaches or suggests these specific features.

In the first place, neither Matsushita nor any of the other cited references at all suggest use of compression strain in the recited gate insulating oxide materials (e.g., titanium oxide, zirconium oxide and hafnium oxide). Quite to the contrary, the primary reference merely provides a general statement of "less strains." It is respectfully submitted that "less strains" found in Matsushita gives no suggestion whatsoever of the claim limitation of "compression strain." Quite to the contrary, Matsushita's goal of providing less strain would actually have the ideal of zero strain. The term "less stains" could be either compression stain or tensile strain, and clearly both types of strain are sought to be minimized by Matsushita since he apparently equates such strain with the undesirable creation of crystal defects.

In effect, Matsushita's teaching of "less strains" actually teaches directly away from the present invention since less strain means an attempt to have no strain, whereas the present claimed invention deliberately introduces compressive strain to achieve the inventive purpose. For the Examiner's convenience, a partial translation of the Matsushita reference is provided herewith. A marked copy of Matsushita is also provided to correlate the partial translation portions with the actual Japanese text in Matsushita. As can be seen in the translated portions 1 and 3 of the attachment, the term "strain" is used, but no teaching whatsoever is found

concerning compression strain. In the translated portion 3, it is specifically stated that excellent electrical properties are provided, and:

> "This seems to be derived from stability of the composition, less strains, no hygroscopicity and small content of charges of Na, K, etc."

As noted above, it is quite clear that Matsushita seeks to have as little strain as possible, whether it be compression strain or tensile strain.

To this end, it is clear that the intended purpose for Matsushita is to substantially eliminate strain to thereby eliminate defects. MPEP 2143.01 specifically provides a section headed "The Proposed Modification Cannot Render the Prior Art Unsatisfactory for its Intended Purpose." As set forth under this section of the MPEP:

> "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

It is respectfully submitted that this would be exactly the situation in the present instance since Matsushita seeks to substantially eliminate all strains, whereas the present claimed invention deliberately introduces compression strain for reduction of leakage current. In other words, the intended purpose of Matsushita (reduction or elimination of all strain) is directly opposite the intended purpose of the present invention (deliberate introduction of compression strain for reducing leakage current). As such, any modification of Matsushita to intentionally provide compression strain as is directly opposite Matsushita's intended purpose, and, accordingly, inappropriate.

The next distinguishing feature regarding the independent claims 17, 18, 20, 24, and 25 is the limitation that the interatomic distances are decreased to suppress

leakage current. In the Office Action, it is stated that this is "an inherent functional property," and, as such, is not given patentable weight. Applicants respectfully submit that this property is anything but inherent. In essence, a given body can have either no strain, tensile strain or compressive strain. Webster's New World Dictionary defines "inherent" as "existing in someone or something as a natural and inseparable quality, characteristic, or right; innate; basic; inborn." In other words, to be inherent is something that is a fundamental property, which cannot be separated from the material. Clearly, the fact that a given material might have compressive strain, no strain or tensile strain provides a situation where compressive strains is not inherent. Quite to the contrary of being inherent, strain is something which is introduced to the material either by an external force or a modification of the internal structure. Therefore, to provide the recited compression strain to decrease interatomic distances to suppress leakage current requires a deliberate modification of the material to achieve this compressive strain. It is respectfully submitted that this is clearly not "an inherent functional property" for the recited gate insulating materials.

It is recognized at the bottom of page 4 of the Office Action that:

> "Matsushita does not specifically describe the newly added limitation so that interatomic distances are decreased to suppress leakage current from flowing through the gate insulators is an inherent functional property."

However, the Office Action goes on to cite the Okada reference as teaching the decrease of interatomic distances to control the shape and quality of recrystallized film. It is respectfully submitted that the teachings of Okada are not appropriate for modifying the Matsushita reference, and, even if the two references were combined,

the result would still not be the claimed invention set forth in the independent claims 17, 18, 20, 24 and 25, or their dependent claims.

In the first place, as noted above, Matsushita's attempt to provide less strains teaches directly away from the recited compression strain to reduce interatomic distances. Therefore, the attempt to modify Matsushita with the teaching of Okada would go directly against the intended purpose of Matsushita, which is prohibited by the above-noted teachings of MPEP 2141.01.

In the second place, the teachings of Okada with regard to interatomic distances are completely different than the purposes defined in the claims of the present invention. As noted above, independent claims 17, 18, 20, 214 and 25 each relate the reduction of interatomic distances to suppression of leakage current. This interrelationship between reduced interatomic distances and suppressed leakage current is completely unrecognized by Okada. Quite to the contrary, Okada seeks to control interatomic distances to attain low stress in crystallization by setting the average interatomic distance to be substantially equal to the average interatomic distance of the single crystal material (e.g., see column 13, lines 23-29 of Okada). For example, column 13, lines 37-55 teaches the control of the interatomic distances during crystallization to suppress stress. Although this may be of general interest, it is absolutely nothing to do with reducing the interatomic distance for suppressing leakage current, as required by each of the present independent claims 17, 18, 20, 24 and 25. Therefore, even if Matsushita could be modified with the teachings of Okada, the end result would be completely different than that defined by the present claims.

In addition to the above points, it is noted that the Matsushita reference teaches a gate insulating film thickness of 1,000 Å (e.g., 100 nm), as set forth in portion 2 of the attached partial English translation. It is noted that such a large thickness is quite unsuitable for a transistor in accordance with the present invention, which as much smaller thickness for the gate insulating film. This large thickness for the gate insulating film in Matsushita serves to make it even more inappropriate for the modification of Matsushita to introduce compressive strain for reducing leakage current.

As discussed above, the primary reference to Matsushita and the secondary reference to Okada completely fail to teach of suggest the essential features defined in each of the independent claims 17, 18, 20, 24 and 25. As such, nothing in the cited secondary reference to VanDover and Lau, which have been referred to primarily for features found in the dependent claims, makes up the for fundamental shortcomings of either of the references to Matsushita or Okada. Therefore, reconsideration and allowance of the independent claims 17, 18, 20, 24 and 25, together with their dependent claims, over the cited combination of references is respectfully requested.

Independent Claims 12, 19 and 22 and Their Dependent Claims.

Each of the independent claims 12, 19 and 22 defines it's own distinguishing features over the cited prior art to Matsushita, Okada, VanDover and Lau discussed above. For example, independent claim 12 defines a combination of features of a channel region in a tensile strain arrangement with a titanium oxide gate insulator having a anatase main crystal structure to inhibit tunneling current caused by the

tensile strain. As such, a relationship is defined between tensile strain in the channel region and the main crystal structure of the titanium oxide as set forth in claim 12 which is completely unsuggested by the cited prior art. As discussed above, the goal of Matsushita is to eliminate strain as much as possible. The purpose of claim 12 is to provide a specific main crystal structure for a titanium oxide gate insulator to inhibit a rise in tunneling current caused by a tensile strain. In other words, the present claim 12 recognizes the existence of tensile strain in a channel region, and accounts for this appropriately with the specific crystal structure of the titanium oxide gate insulator. This concept of inhibiting an undesirable effect of tensile strain in a channel region is completely unrecognized and unsolved by any of the cited prior references.

Turning to independent claim 19, this teaches the titanium oxide having a rutile crystal structure and a specific relationship between the thermal expansion coefficient of the gate electrode being greater than the linear expansion coefficient of the titanium oxide gate insulator. Again, the cited references to Matsushita, Okada, VanDover and Lau completely fail to recognize this interrelationship between the material used for the titanium gate insulator (that is, having a rutile crystal structure) and the claimed relationship between the thermal expansion coefficient of the gate electrode and the linear expansion coefficients of the titanium oxide gate insulator. Therefore, it is respectfully submitted that claim 19 defines over the cited prior art.

Claim 22 defines a first MOS transistor having a gate insulator of high permittivity for high speed in conjunction with a second MOS transistor having a gate insulator of silicon oxide to resist high gate voltages. It is respectfully submitted that none of the cited prior art teaches or suggests this particular relationship between